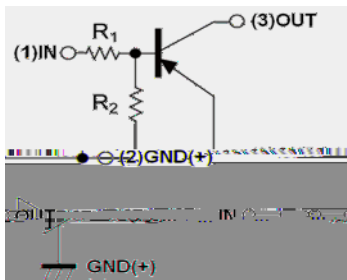
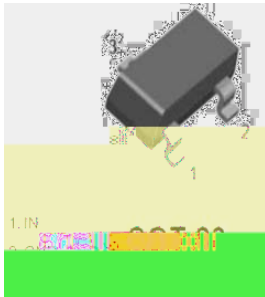




PNP Digital Transistors (Built-in Resistors)



Features

- Moisture sensitivity level 1
- Halogen free and RoHS compliant
- Surface mount package ideally suited for automatic insertion

Application

- Signal amplification
- Switching circuit

Mechanical data

- Package** SOT-23
- Terminals** Tin plated leads, solderable per J-STD-002 and JEDEC22-B102

Maximum Ratings (T_a=25 Unless otherwise specified)

Item	Symbol	Unit	Conditions	Value
Input voltage	V _I	V		-3 V to +1 V
Output current	I _O	mA		-10 mA
Power dissipation	P _D	mW		100
junction temperature	T _J	°C		-55 to +150
Storage temperature	T _{STG}	°C		-55 to +150



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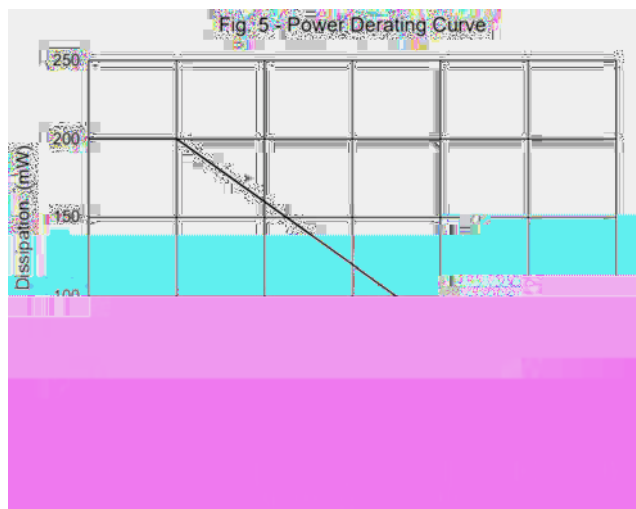
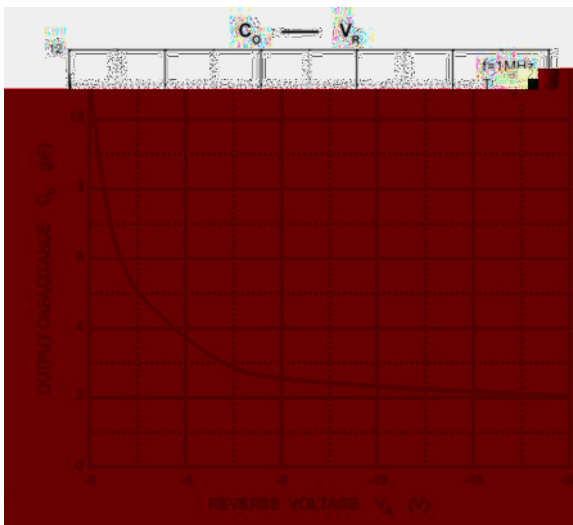
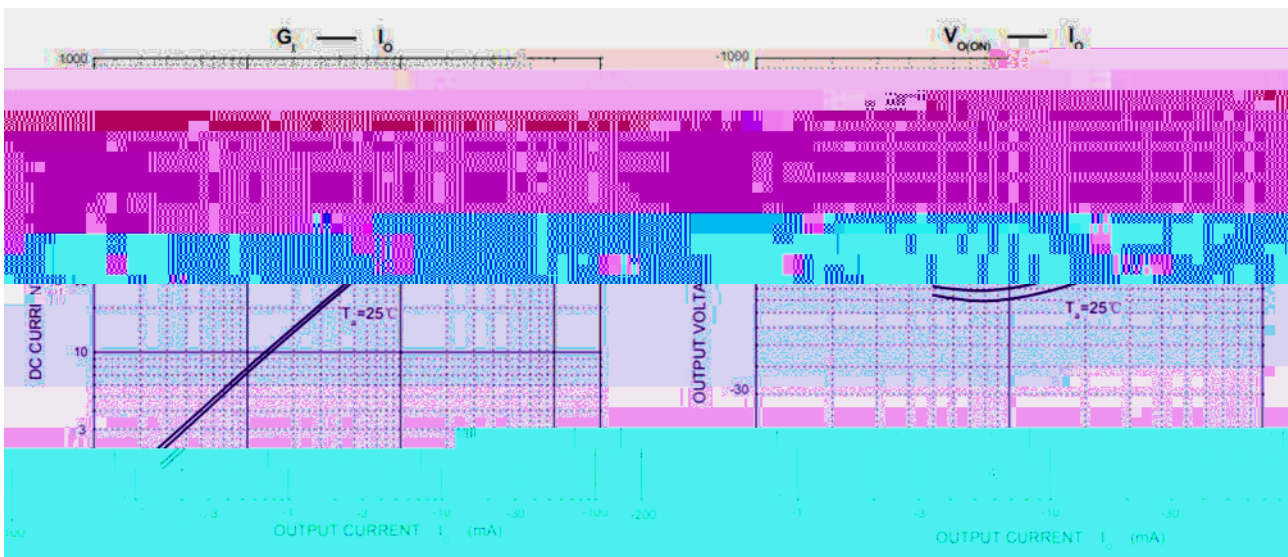
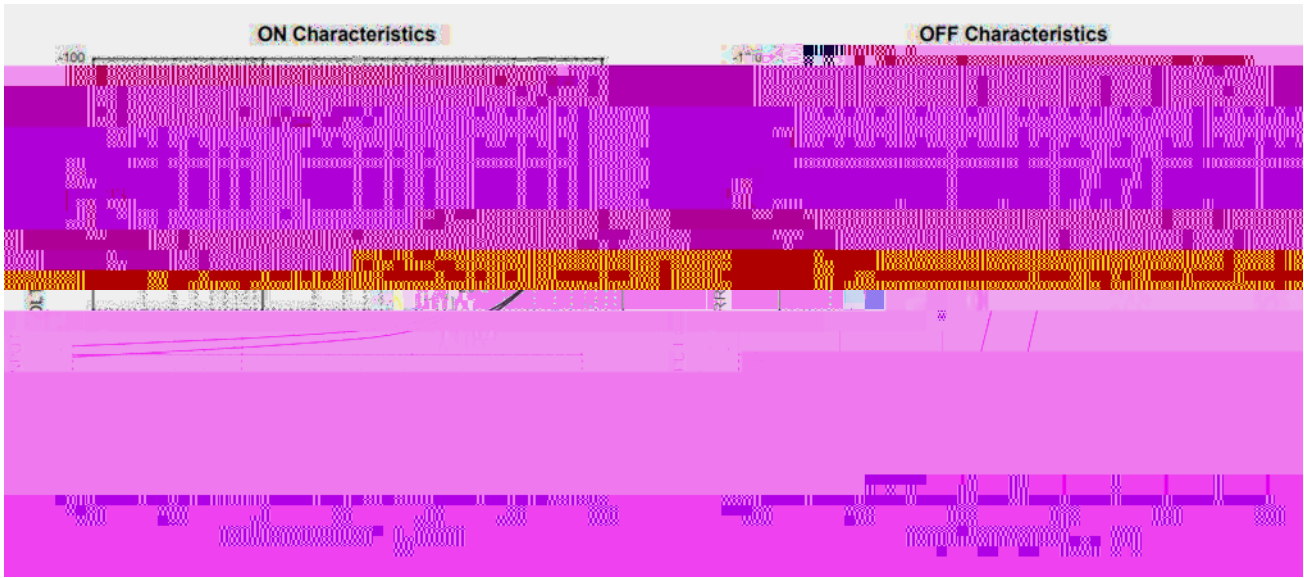
RoHS
COMPLIANT

Electrical Characteristics (T_a=25 Unless otherwise specified)

Item	Symbol	Unit	Conditions	Min	Typ	Max
Input voltage	V _{I(off)}	V	V _{CC} =-5V, I _O =-100uA	-0.5		
	V _{I(on)}	V	V _O =-0.3V, I _O =-20mA			-3.0
Output voltage	V _{O(on)}	V	I _O / I _I = -10mA / -0.5 mA			-0.3
Input current	I _I	mA	V _I =-5V			-1.8
Output current	I _{O(off)}	uA	V _{CC} =-50V, V _I =0			-0.5
DC current gain	G _I					

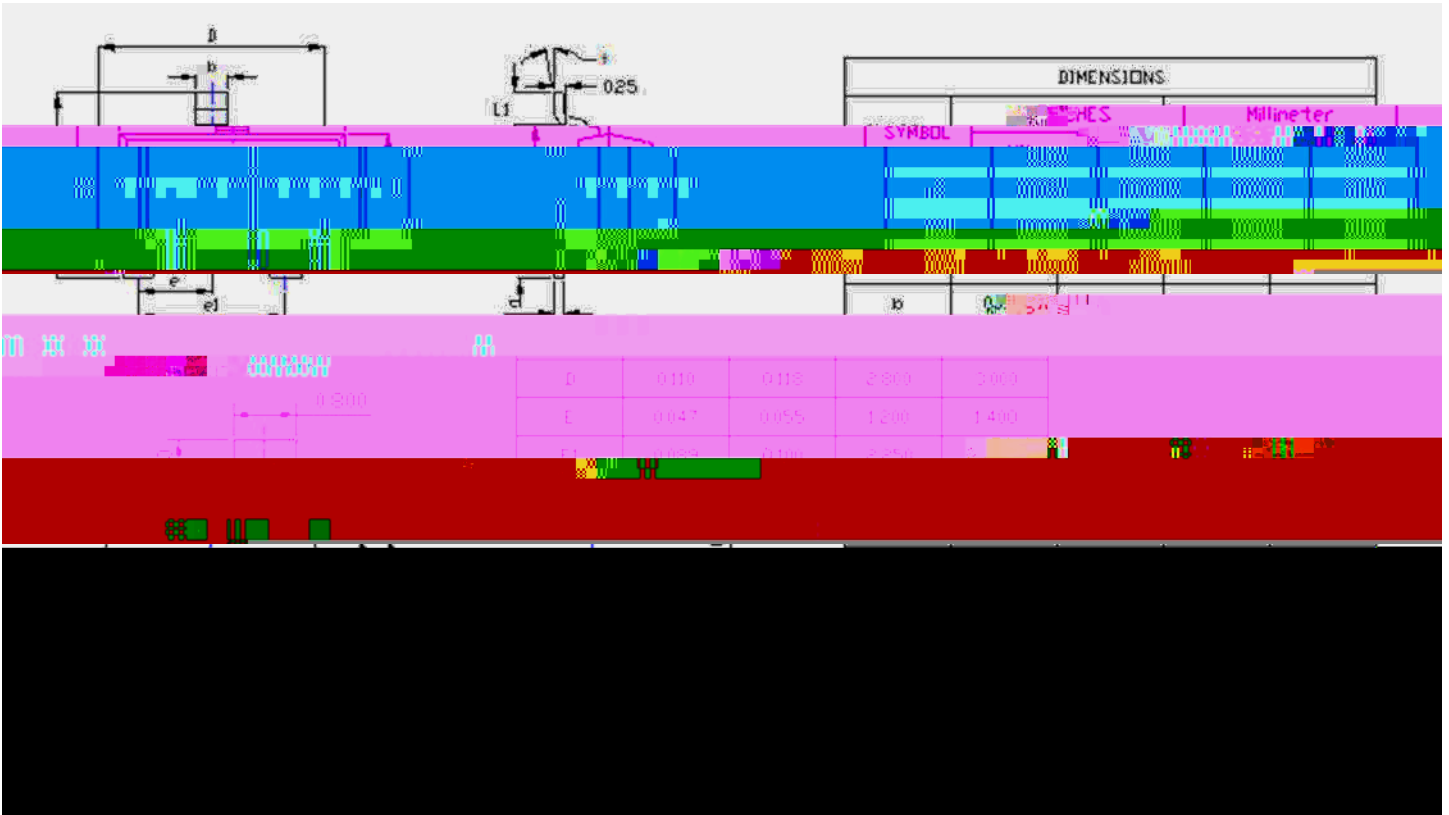


Characteristics





Outline Dimensions



Note:

- All dimensions are in millimeters (mm) unless otherwise specified.

All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.

尺寸B不包括单边最大为0.100 mm的引脚凸出部分

Dimensions A and B shall be measured on the maximum diameter of the leads.

尺寸A和B是在引脚最大直径处测量的。

7. Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.

成型引脚应为一平面，共面性最大为0.076 mm。

8. ★ It is the key size.
[★ 标记为关键尺寸]



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