N-Channel Enhancement Mode Field Effect Transistor

Product Summary

● V_{DS}	100V
● I_D	45A
● $R_{DS(ON)}$(at V_{GS}=10V)	12.5mΩ
● $R_{DS(ON)}$(at V_{GS}=4.5V)	16mΩ
● 100% EAS Tested	

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25 -	I_D	8	A
	T_A=100 -		5	
	T_C=25 -		45	
	T_C =100 -			

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=150 -	-	-	100	
Gate-Body Leakage Current	I_{GSS}					

GGS

G DS

Typical Electrical and Thermal Characteristics Diagrams

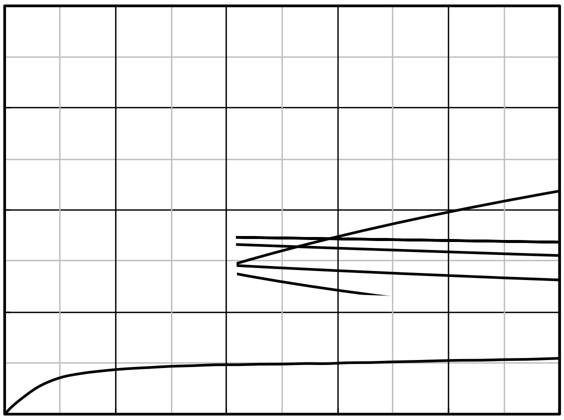


Figure 1. Output Characteristics

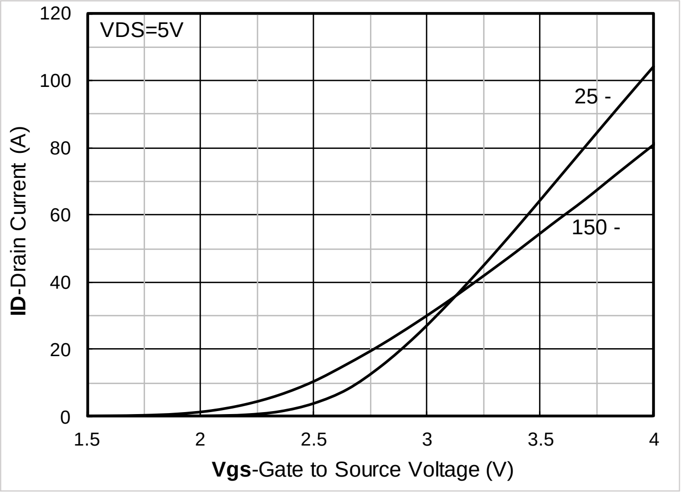


Figure 2. Transfer Characteristics

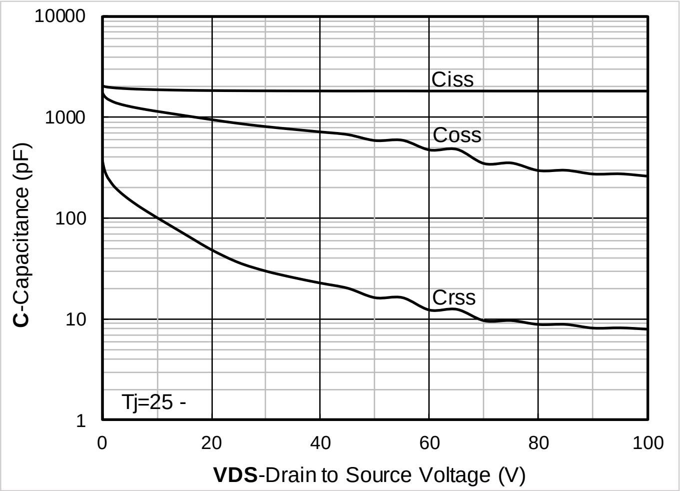


Figure 3. Capacitance Characteristics

Figure 4. Gate Charge

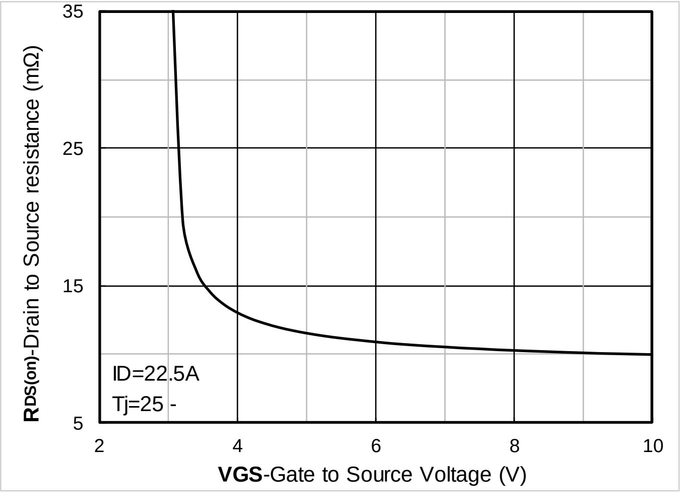


Figure 5. On-Resistance vs Gate to Source Voltage

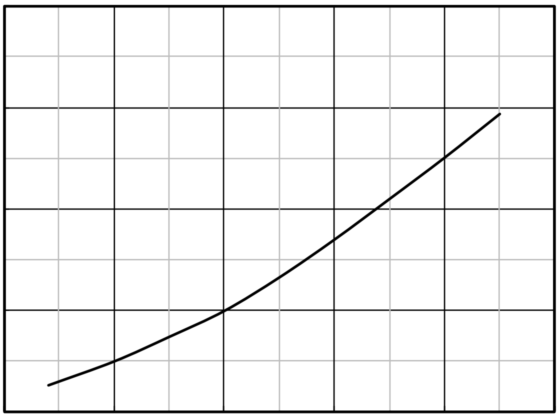


Figure 6. Normalized On-Resistance

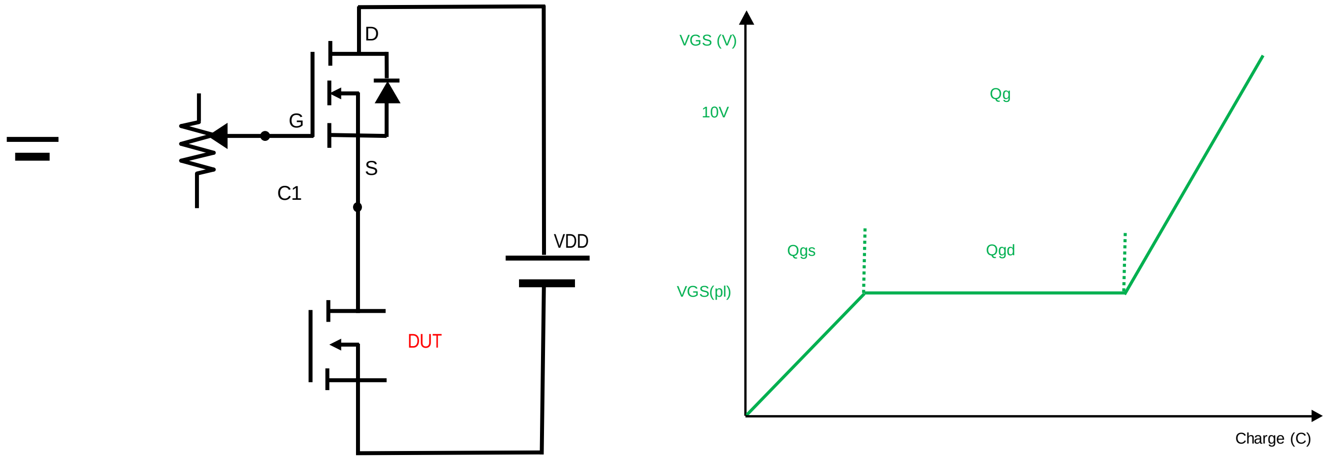


Figure B. Gate Charge Test Circuit & Waveform

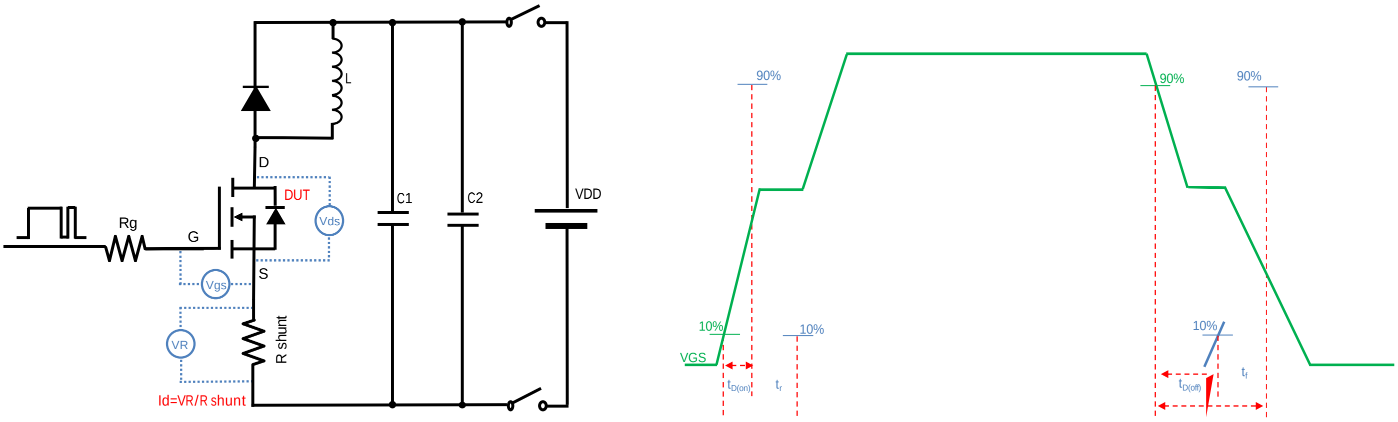
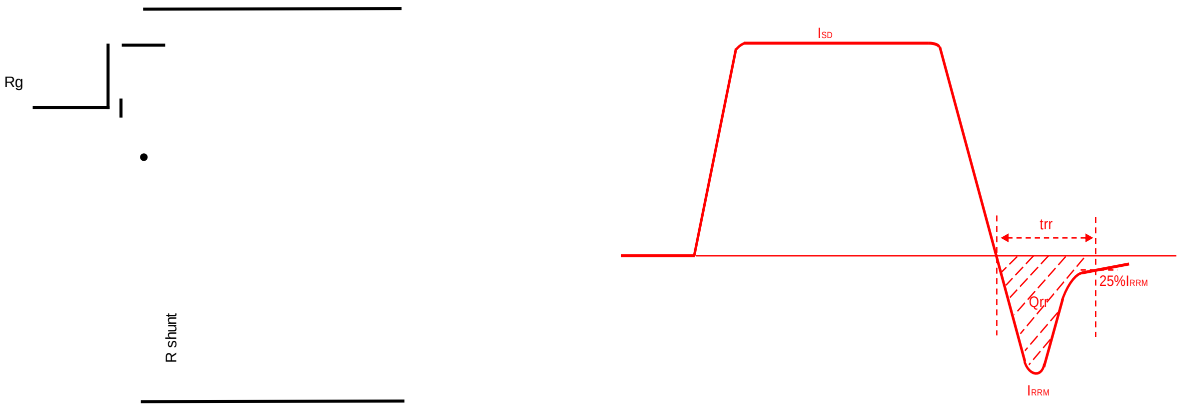
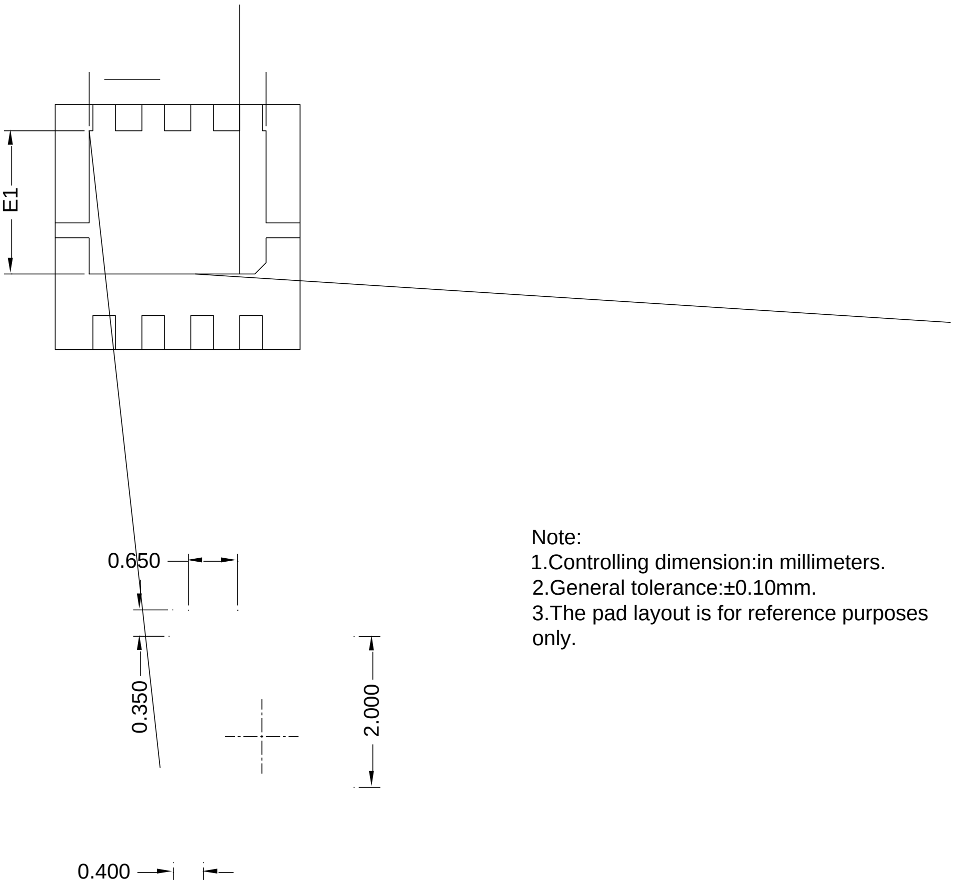


Figure C. Resistive Switching Test Circuit & Waveform



■ DFN3333-8L-A-0.8MM Package information



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.