N-Channel Enhancement Mode Field Effect Transistor

Product Summary

● V_{DS}	40V
● I_D	20A
● $R_{DS(ON)}$(at V_{GS}=10V)	15.0mΩ
● $R_{DS(ON)}$(at V_{GS}=4.5V)	20.0mΩ
● 100% EAS Tested	

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching applicati
- Uninterruptible power su
- DC-DC convertor
- 12V Automotive systems

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	M
YJQ20N04AQ	F1	Q

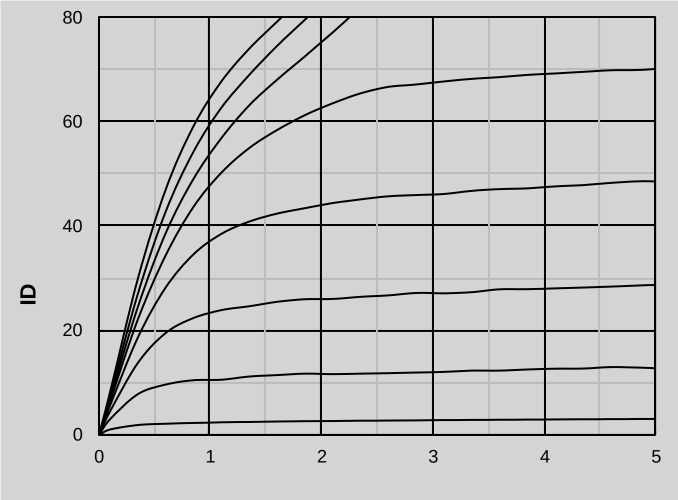
■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	T_C=25	I_D	20	A
	T_C =100		17	
Pulsed Drain Current [A]		I_{DM}	80	[redacted]
Avalanche energy [B]		EAS	[redacted]	[redacted]
Total Power Dissipation [C]	T_A=25	P_D	[redacted]	[redacted]
	T_C=25		[redacted]	[redacted]
Thermal Resistance Junction-to-Case	Steady-State	$R_{θJC}$	5.9	/W

■ **Electrical Characteristics** (T$_J$=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units

■Typical Electrical and Thermal Characteristics Diagrams



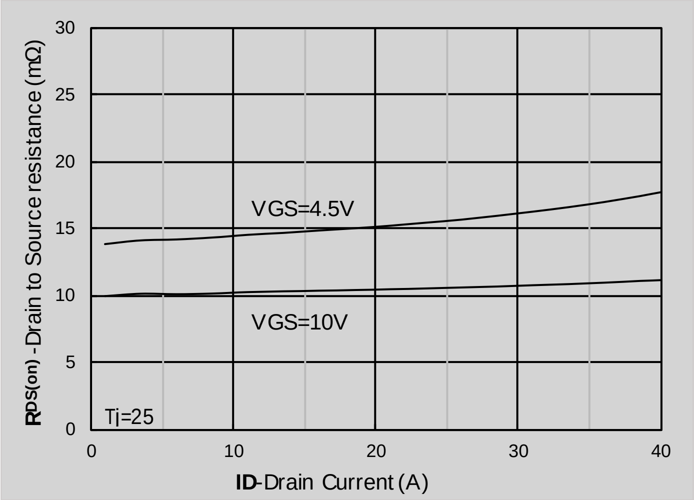


Figure 7. RDS(on) VS Drain Current

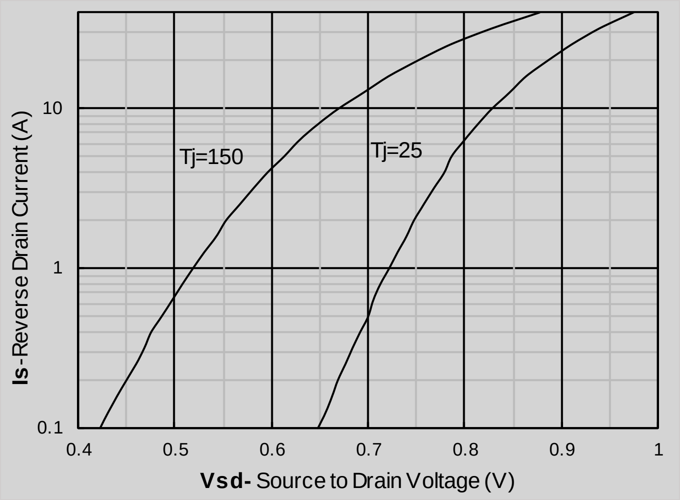
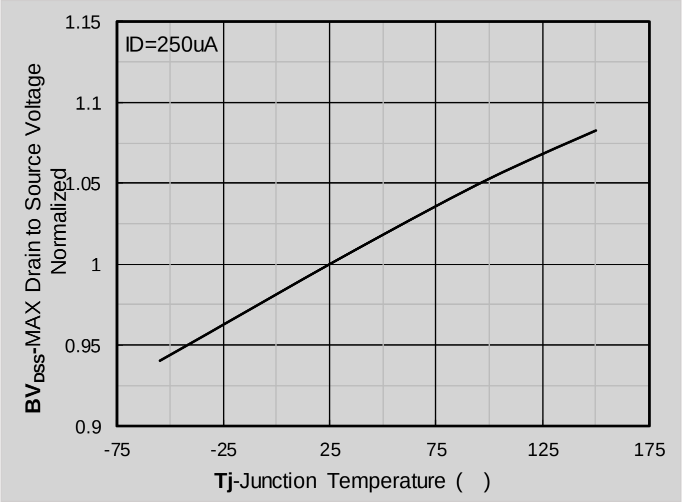


Figure 8. Forward characteristics of reverse diode



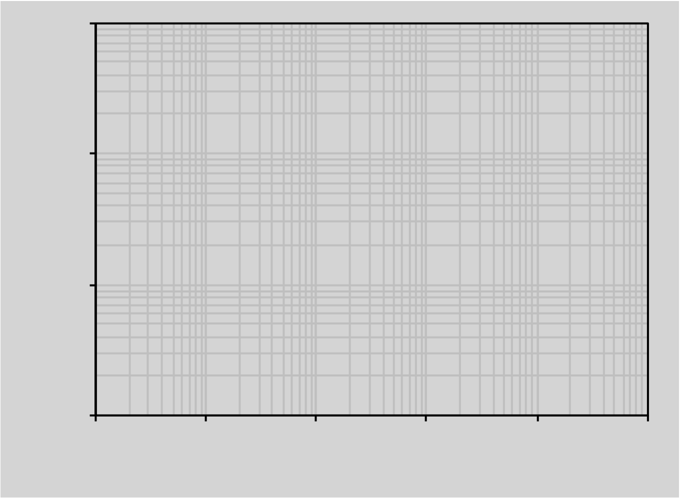
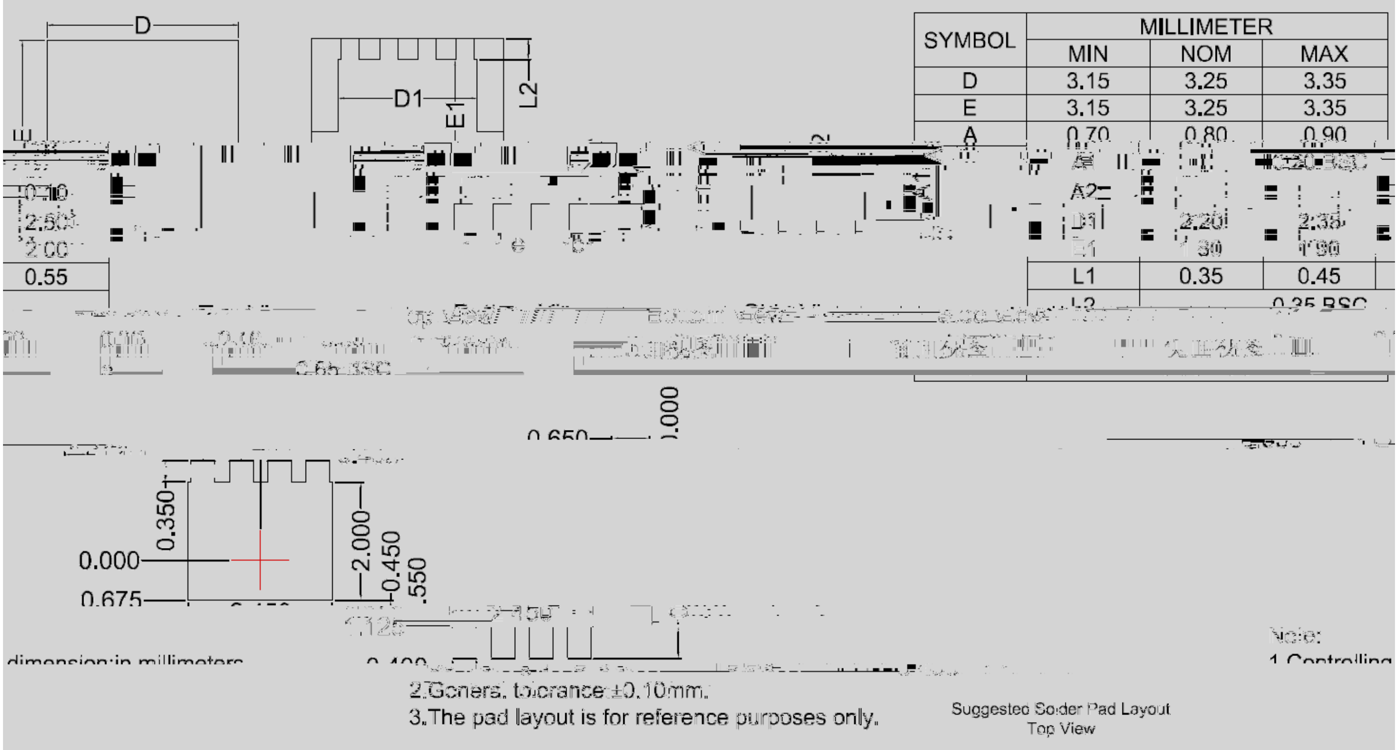


Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area

■DFN3333-8L Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	[illegible]	[illegible]	[illegible]
A2	[illegible]	[illegible]	[illegible]
D1	[illegible]	2.20	2.35
E1	[illegible]	1.80	1.90
L1	0.35	[illegible]	0.45
L2	0.35 BSC		

Note:

1.Controlling dimension:in millimeters

2.General tolerance:±0.10mm.

3.The pad layout is for reference purposes only.

Disclaimer

The information presented in this document is for reference onl