N-Channel Enhancement Mode Field Effect Transistor

Product Summary

ð V_{DS} 100V
ð I_D 4.0A
ð $R_{DS(ON)}$(at V_{GS}= 10V) 110mohm
ð $R_{DS(ON)}$(at V_{GS}= 4.5V) 120mohm

General Description

ð Trench Power MV MOSFET technology
ð Excellent package for heat dissipation
ð High density cell design for low $R_{DS(ON)}$
ð Epoxy Meets UL 94 V-0 Flammability Rating
ð Halogen Free

Applications

ð DC-DC Converters
ð Power management functions

ý Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	Ñ20	V
Drain Current	T_A=25	I_D	4	A
	T_A=70		3.2	
Pulsed Drain Current [A]		I_{DM}	16	A
Total Power Dissipation @ T_A=25		P_D	2.5	W
Thermal Resistance Junction-to-Ambient [B]		R_{dJA}	50	/ W
Thermal Resistance Junction-to-Case		R_{dJC}	16	/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

ý Ordering Information (Example)

	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJM04N10A	F2	1004	2500	/	40000	13ñ reel
			2500	5000	25000	13ñ reel

y′ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250εA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	εA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= Ñ20V, V_{DS}=0V			Ñ100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250εA	1.1	1.8	3.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=4A		95	110	mq
		V_{GS}= 4.5V, I_D=3.2A		100	120	
Diode Forward Voltage	V_{SD}	I_S=4A,V_{GS}=0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I_S				4	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ		1070		pF
Output Capacitance	C_{oss}			33		
Reverse Transfer Capacitance	C_{rss}			30		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=10A		26		nC
Gate-Source Charge	Q_{gs}			5.4		
Gate-Drain Charge	Q_{gd}			5.8		
Reverse Recovery Charge	Q_{rr}	I_F=10A, di/dt=100A/us		30.1		
Reverse Recovery Time	t_{rr}			40		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V,R_L=6.4q R_{GEN}=3q		7		
Turn-on Rise Time	t_r			24		
Turn-off Delay Time	$t_{D(off)}$			24		
Turn-off fall Time	t_f			31		

A. Pulse Test: Pulse Width ≤ 300us,Duty cycle ≤ 2%.

B. R_{dJA} is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R_{dJL} is guaranteed by design, while R_{dJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

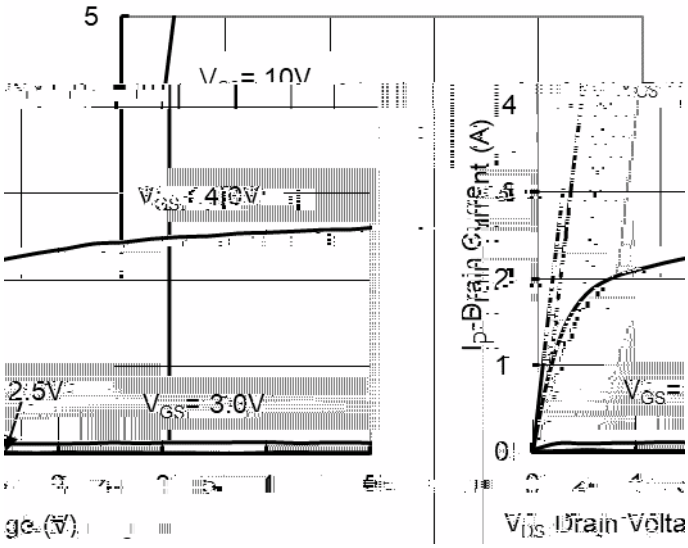


Figure 1. Output Characteristics

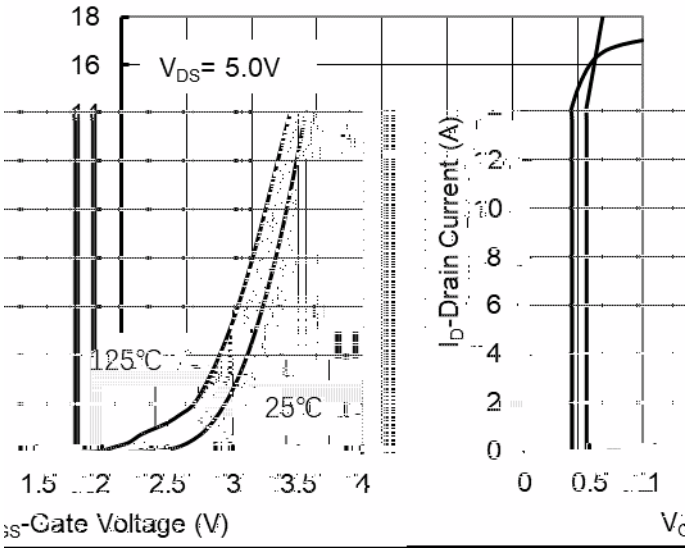


Figure 2. Transfer Characteristics

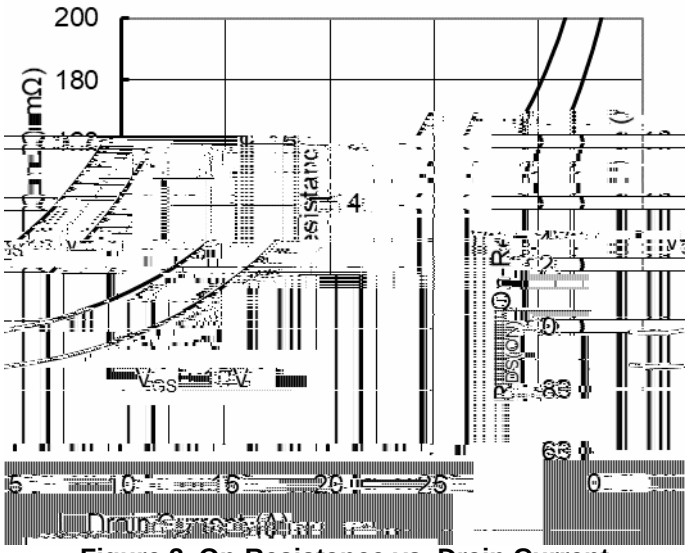
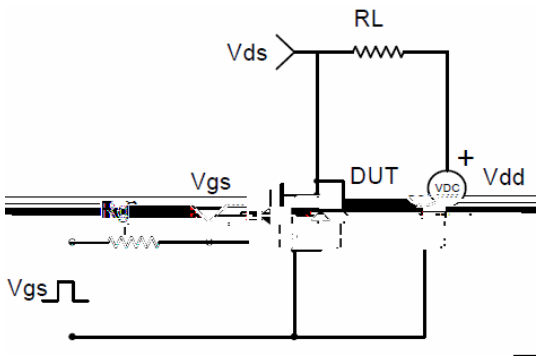


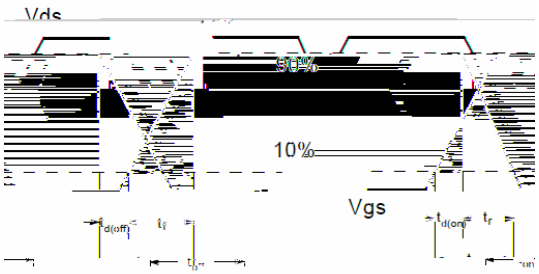
Figure 3. On-Resistance vs. Drain Current and Gate Voltag

)LJXUH   6DIH 2SHUDWLRQ $UHD

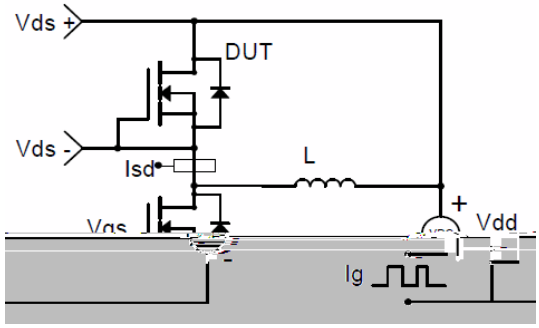
)LJXUH   0D[LPXP &RQWLQXRXV 'UDL
YV $PELHQW 7HPSHUDWXUH

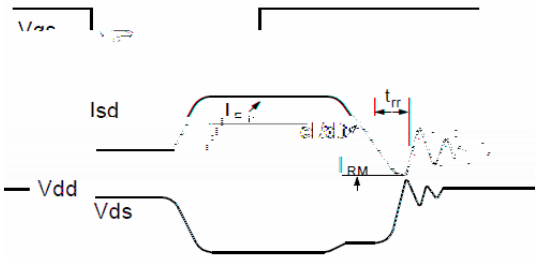
)LJXUH   1RUPDOL]HG 0D[LPXP 7UDQVLHQW 7KHUPDO ,PSHGDQFH



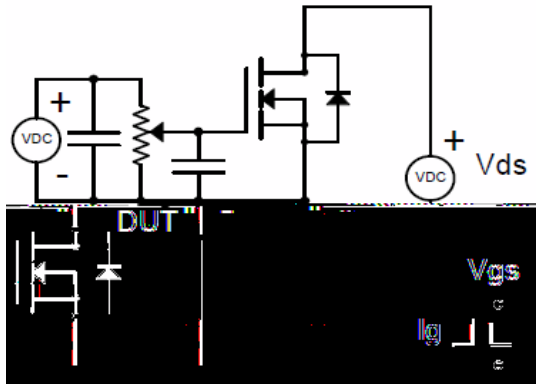


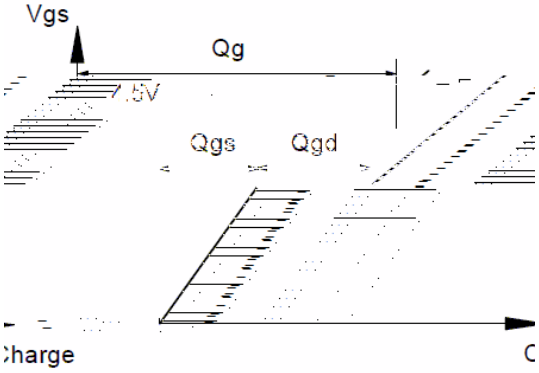
Resistive Switching Test Circuit & Waveforms



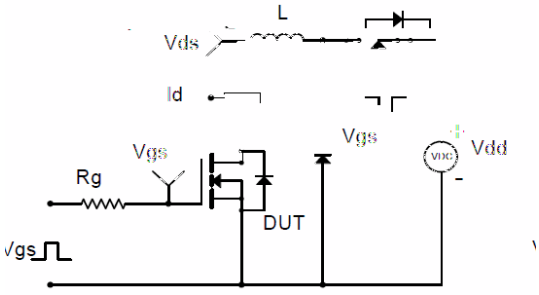


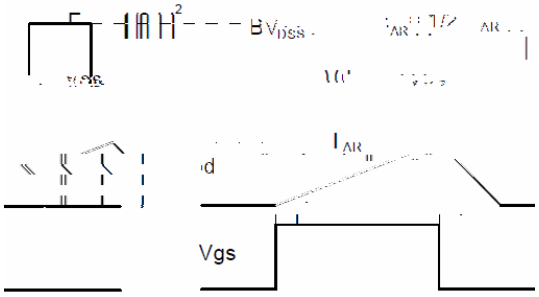
Diode Recovery Test Circuit & Waveforms





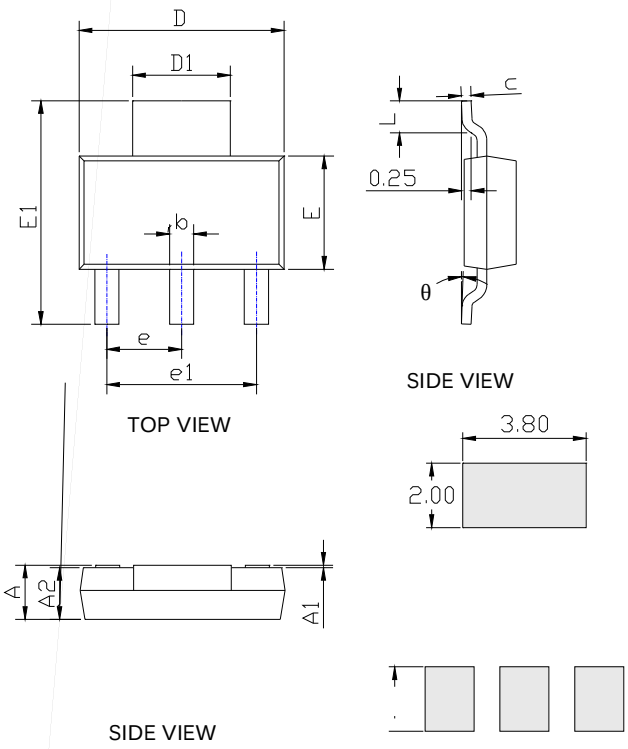
Gate Charge Test Circuit & Waveform





SOT-223 Package information

TYPE B:



DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.060	0.071	1.520	1.800
A1	0.000	0.004	0.000	0.100
A2	0.059	0.067	1.500	1.700
b	0.026	0.032	0.660	0.820
c	0.010	0.014	0.250	0.350
D	0.244	0.252	6.200	6.400
D1	0.114	0.122	2.900	3.100
E	0.130	0.146	3.300	3.700
E1	0.269	0.278	6.830	7.070
e	0.091BSC		2.300BSC	
e1	0.177	0.185	4.500	4.700
L	0.035	0.045	0.900	1.150
θ	0°	10°	0°	10°

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