P-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	-60V
I_D	-40A
$R_{DS(ON)}$(at V_{GS}=-10V)	25 mohm
$R_{DS(ON)}$(at V_{GS}=-4.5V)	30 mohm

100% EAS Tested
100% V_{DS} Tested

General Description

Split gate trench MOSFET technology
Low $R_{DS(on)}$ & FOM
Low Crss
Extremely low switching loss
Excellent stability and uniformity
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

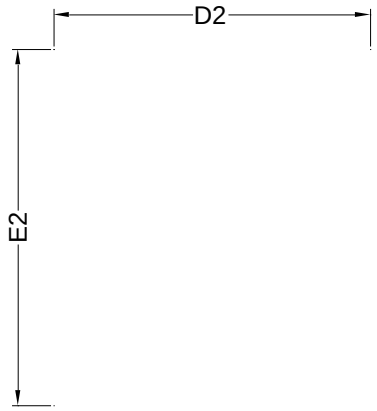
Applications

Load Switch
Industrial DC/DC Conversion Circuits

Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}		

PDFN5060-8L-B-1.1MM



Top View

Bottom View

Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1			

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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