N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	30V
I_D	50A
$R_{DS(ON)}$(at V_{GS}= 10V)	7.3mohm
$R_{DS(ON)}$(at V_{GS}= 4.5V)	11.5mohm

100% EAS Tested

100% V_{DS} Tested

General Description

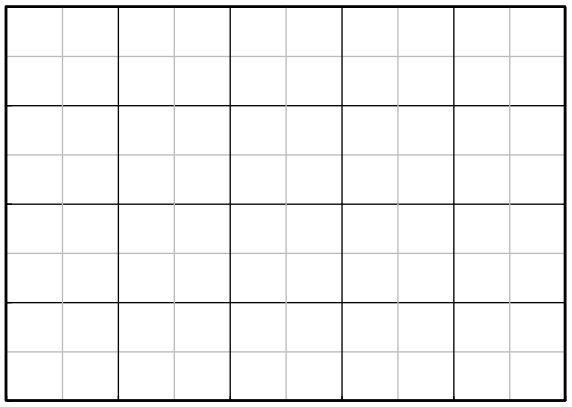
Excellent package for heat dissipation

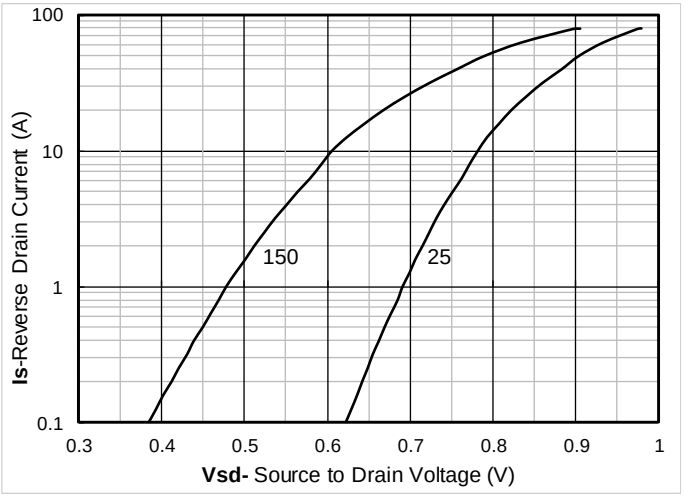
High density cell design for low $R_{DS(ON)}$

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V			1	
		V_{DS}=30V,V_{GS}=0V, Tj=150			100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= 20V, V_{DS}=0V			100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250	1.0	1.5	2.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=15A		5.4	7.3	m
		V_{GS}= 4.5V, I_D=15A		9.5	11.5	
Diode Forward Voltage	V_{SD}	I_S=15A,V_{GS}=0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I_S				50	A
Gate resistance	R_G	f=1MHz		4		
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V,f=1MHZ		1015		pF
Output Capacitance	C_{oss}			201		
Reverse Transfer Capacitance	C_{rss}			164		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=20V,I_D=20A		23.6		nC
Gate-Source Charge	Q_{gs}			3.9		
Gate-Drain Charge	Q_{gd}			7		
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=100A/us		0.2		
Reverse Recovery Time	t_{rr}			5		
Turn-on Delay Time	$t_{D(on)}$					ns

V_{GS}




100
10
1
0.1
Is-Reverse Drain Current (A)
150
25
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Vsd- Source to Drain Voltage (V)

Figure

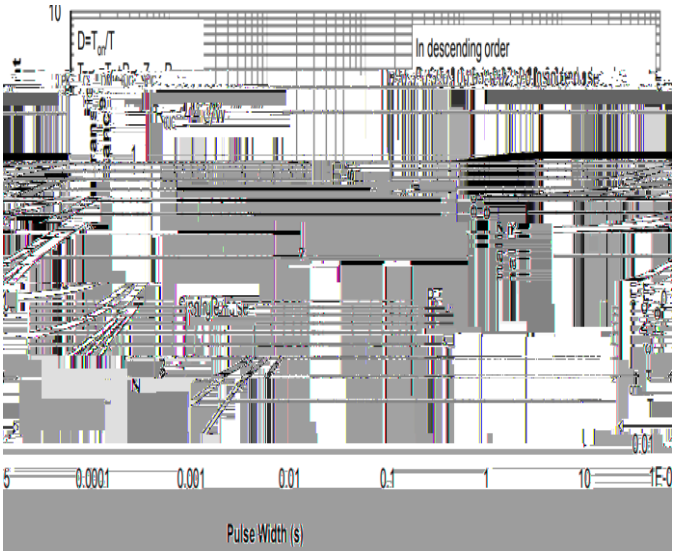


Figure 13. Normalized Maximum Transient Thermal Impedance

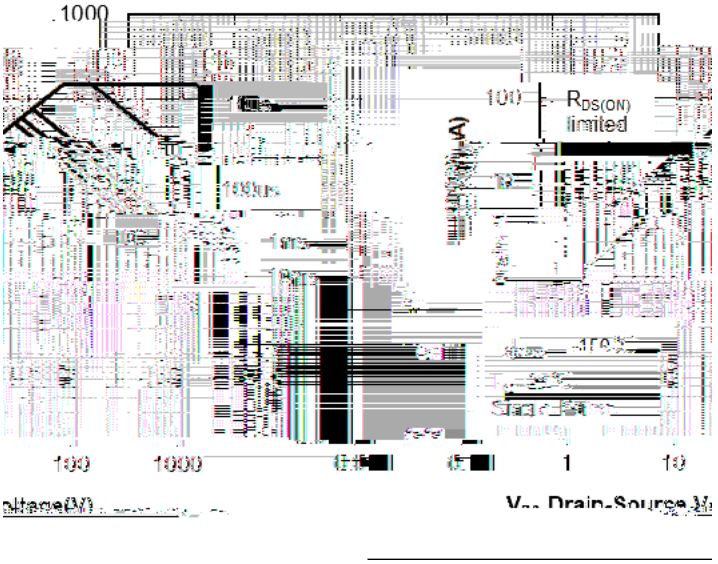
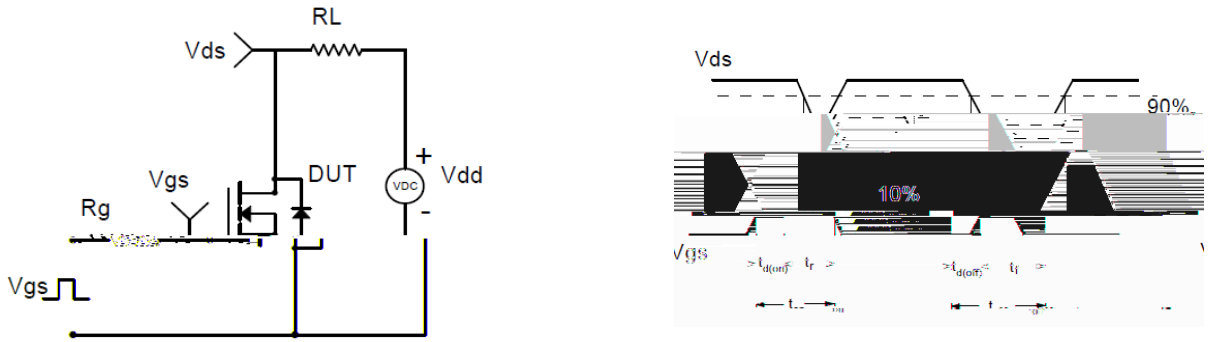
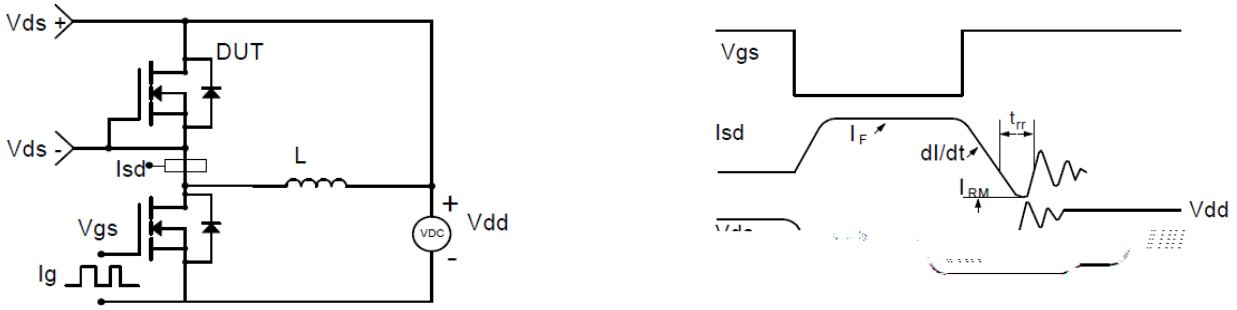


Figure 14. Safe Operation Area

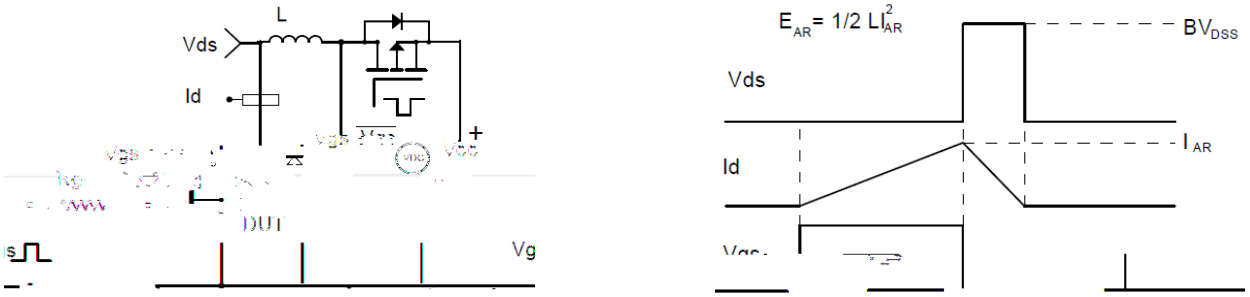


Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

YJD50N03A

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