N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	650V
I_D	11A
$R_{DS(ON)}$(at V_{GS}=10V)	380m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Super Junction High Voltage MOSFET technology
Low $R_{DS(ON)}$ & FOM
Extremely low switching loss
Excellent stability and uniformity
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

Server power
Charger
PD Adapter

Absolute Maximum Ratings (T_A=25

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D	650	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	-	-	1	
		V_{DS}=650V, V_{GS}=0V, Tj=150	-	-	100	

Typical Electrical and Thermal Characteristics Diagrams

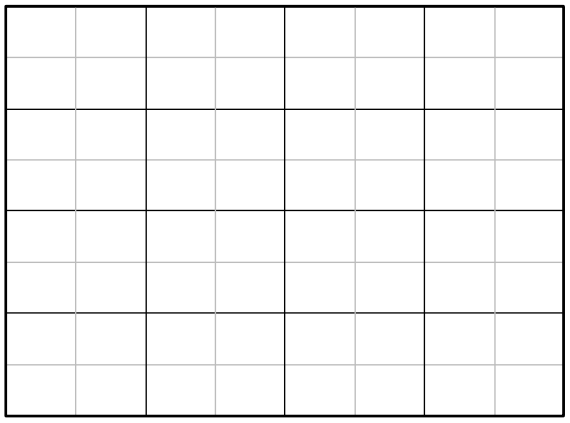

Figure 1. Output Characteristics

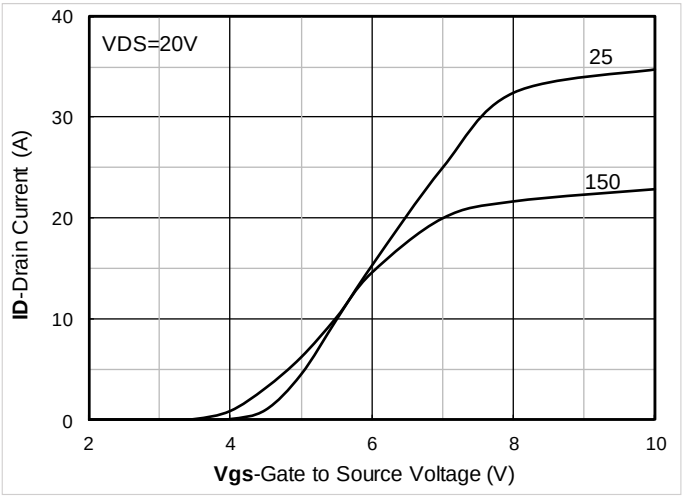

Figure 2. Transfer Characteristics

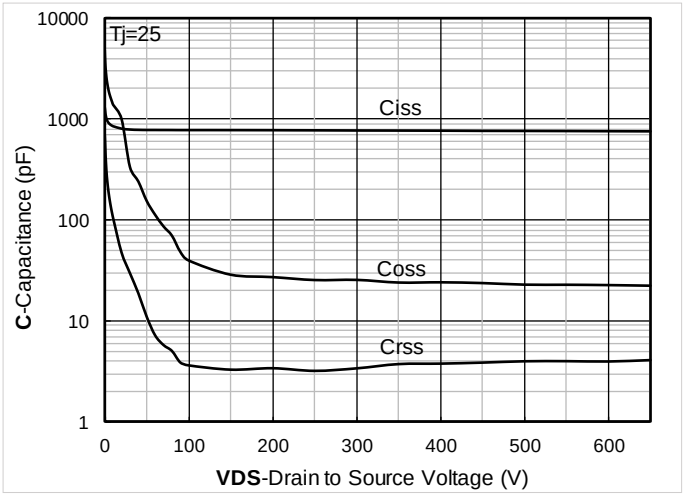

Figure 3. Capacitance Characteristics

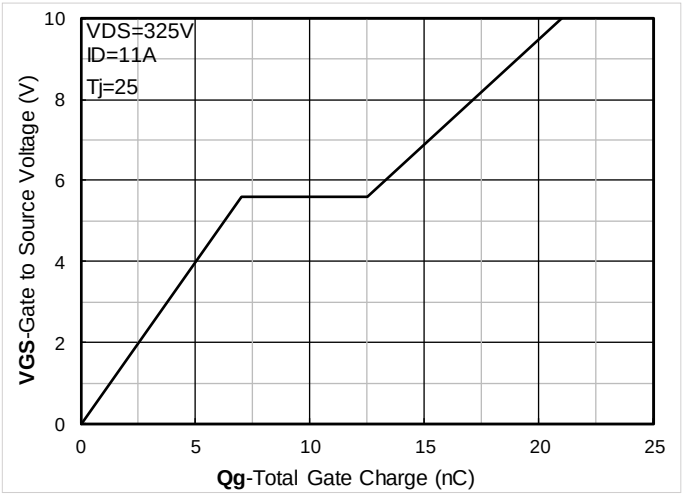

Figure 4. Gate Charge

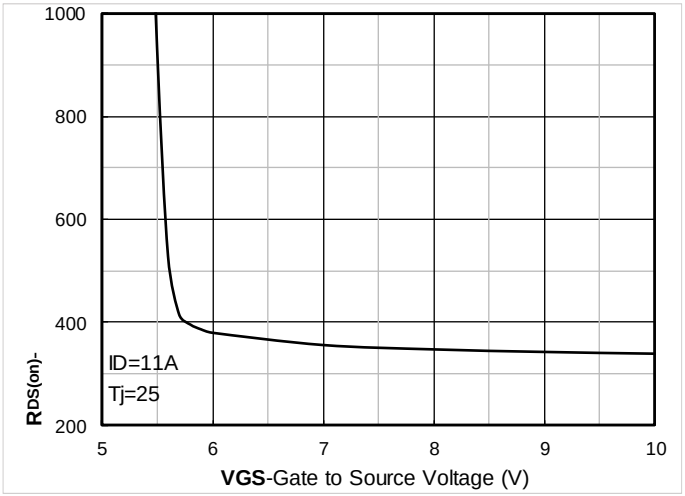

Figure 5. On-Resistance vs Gate to Source Voltage

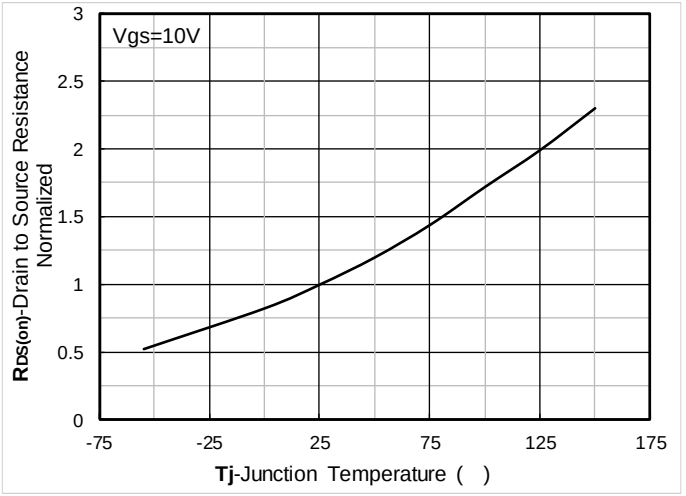

Figure 6. Normalized On-Resistance

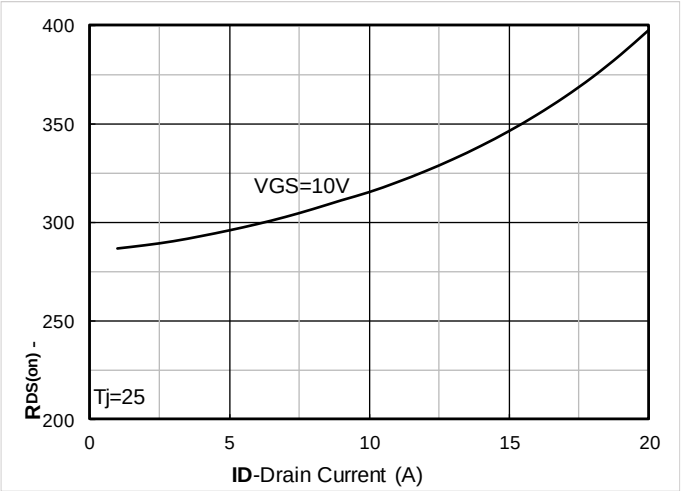

Figure 7. $R_{DS(on)}$ VS Drain Current

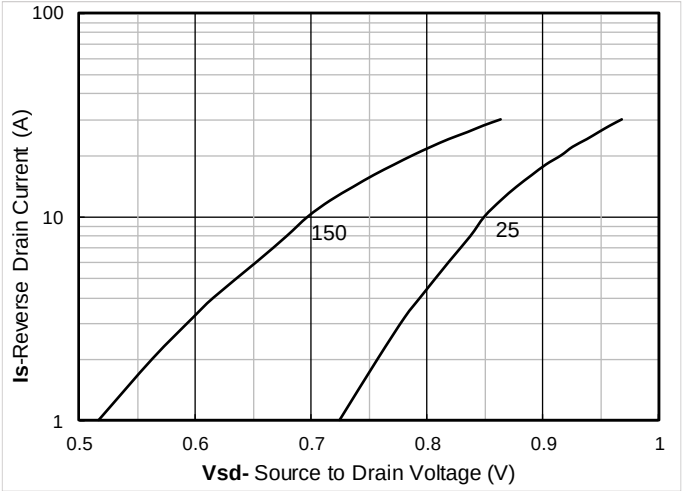

Figure 8. Forward characteristics of reverse diode

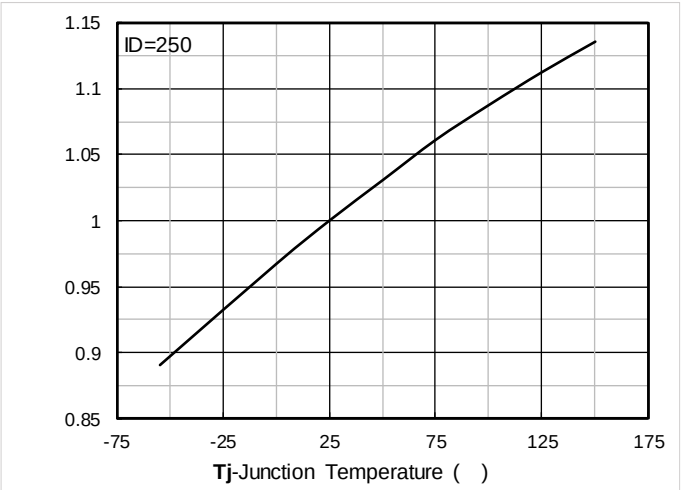

Figure 9. Normalized breakdown voltage

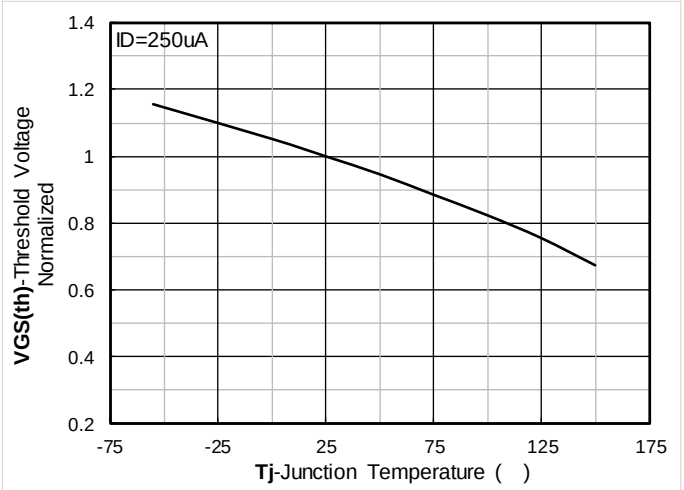

Figure 10. Normalized Threshold voltage

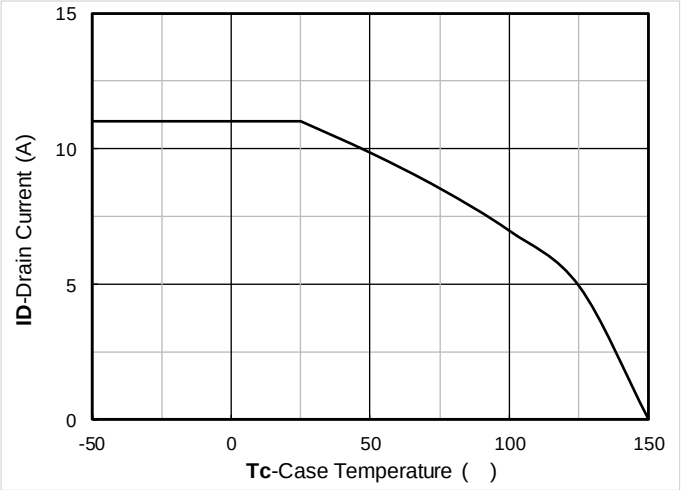

Figure 11. Current dissipation

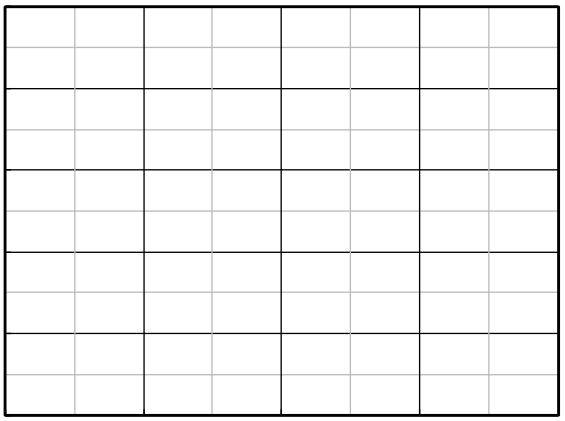

Figure 12. Power dissipation

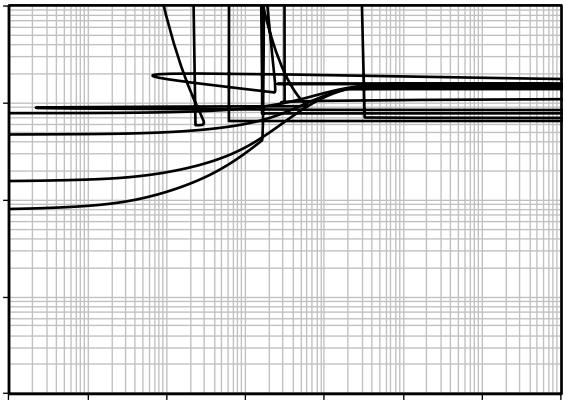

Figure 13. Maximum Transient Thermal Impedance

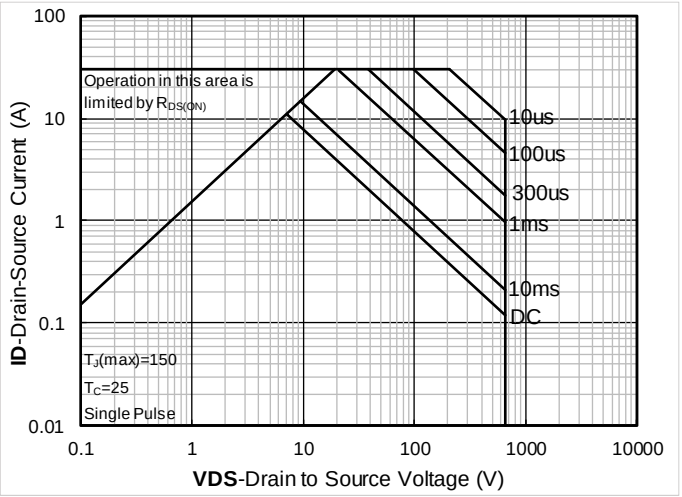

Figure 14. Safe Operation Area

Test Circuits & Waveforms

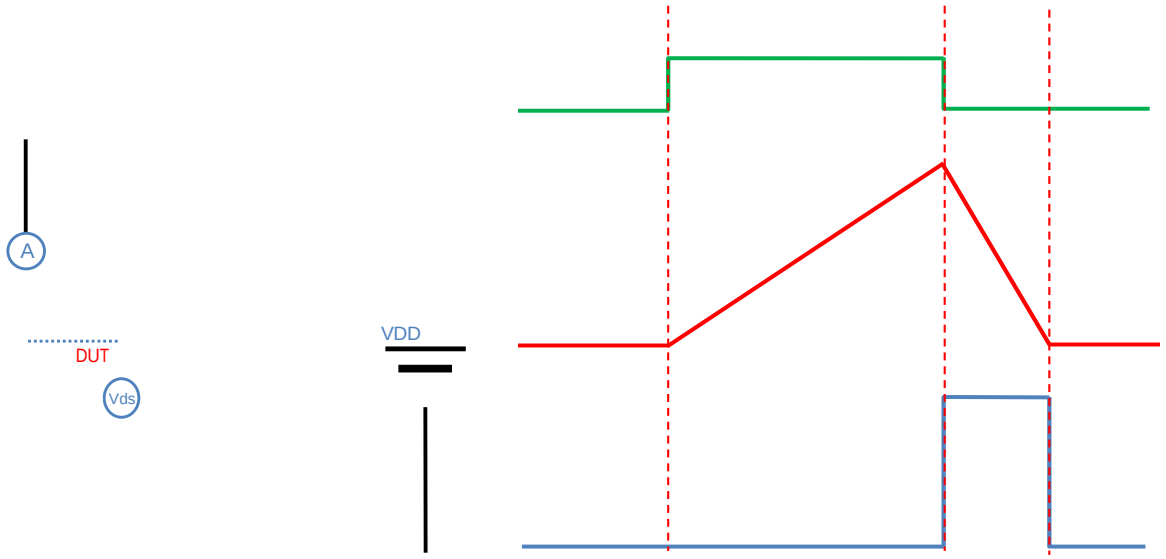

Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

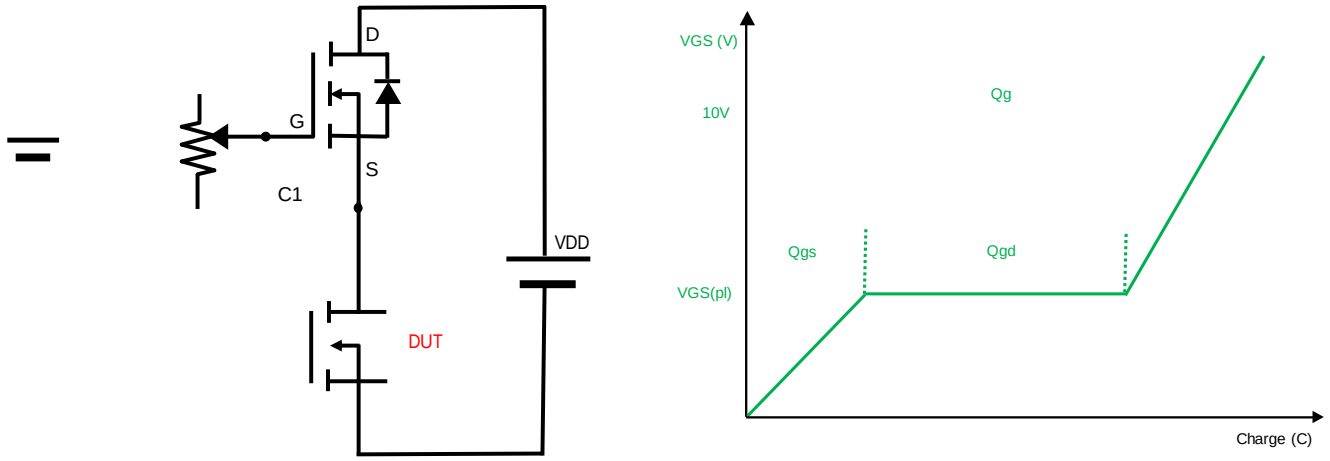

Figure B. Gate Charge Test Circuit & Waveform

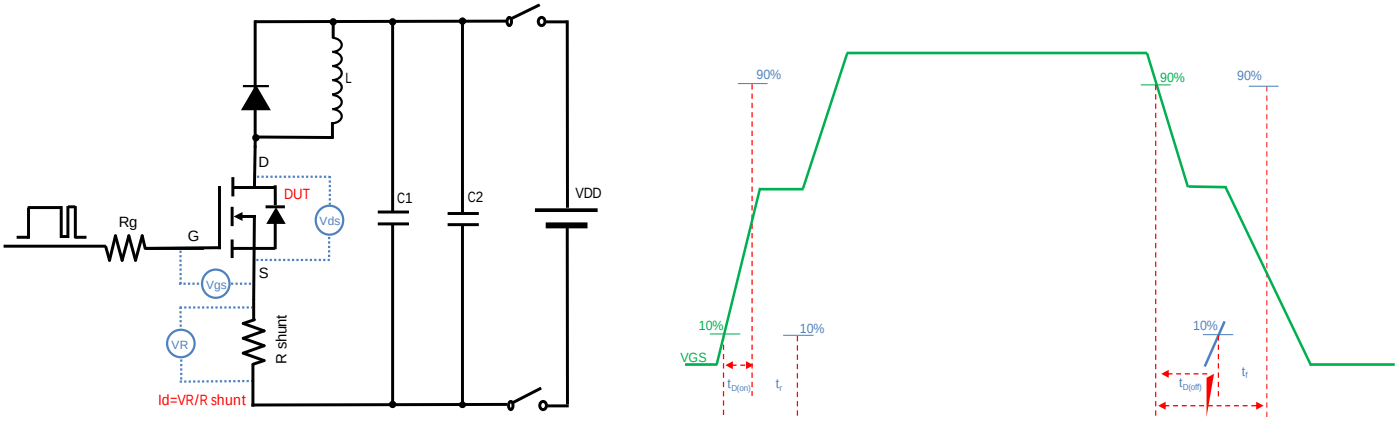

Figure C. Resistive Switching Test Circuit & Waveform

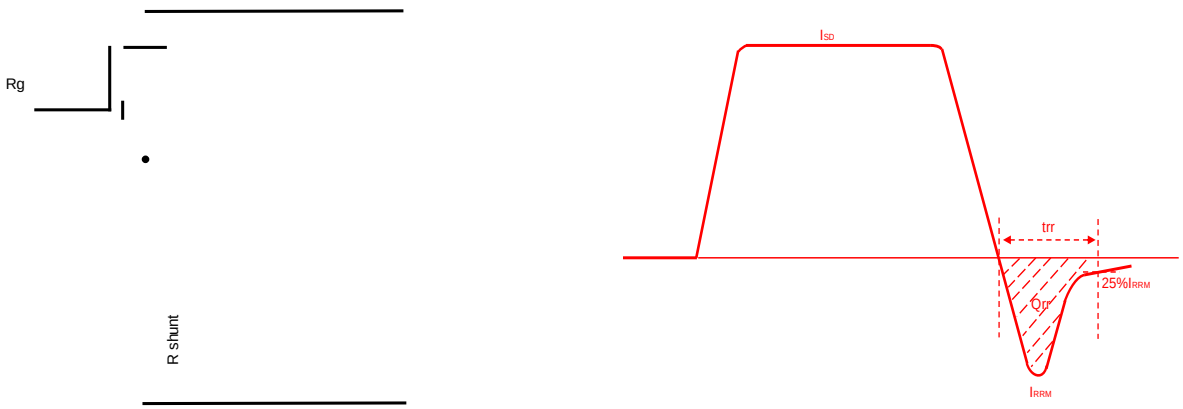

Figure D. Diode Recovery Test Circuit & Waveform

TO-252-B

YJD11C65HJ