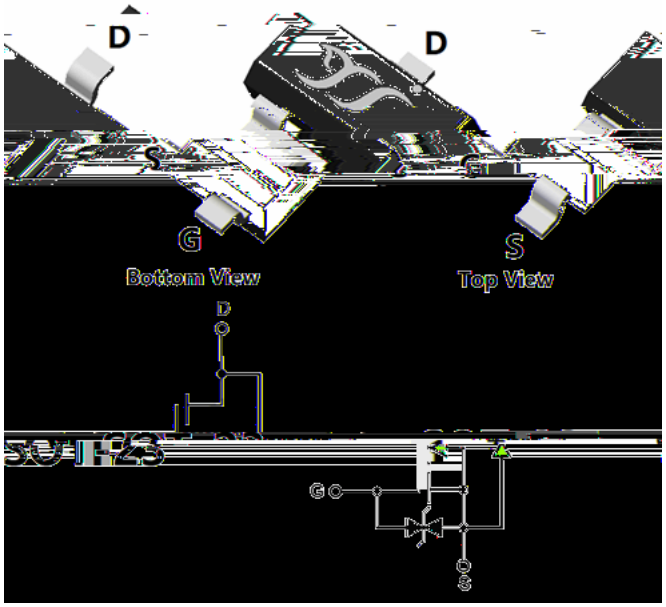
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 50V
- I_D 0.22A
- $R_{DS(ON)}$(at V_{GS}=10V) 1.6Ω
- $R_{DS(ON)}$(at V_{GS}=4.5V) 2.5Ω
- $R_{DS(ON)}$(at V_{GS}=2.5V) 3.8Ω
- Gate-Source ESD Rating Up to 1.5KV (HBM)

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix “Q” means AEC-Q101 qualified

Applications

- Power Management Functions
- Load switch
- DC-DC convertor

■ Absolute Maximum Ratings (T_J=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	50	V
Gate-source Voltage		V_{GS}	±20	V
Continuous Drb	T Đ	‘ `v φ. T l ҽMԓ D p τ ɔ Mϰ φ D rent		
	$_C$=25 , t_p=100μs	I_{DM}	1	A
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25		R

		$_{\theta JA}$	-	202	/W

■ Ordering Information (Example)

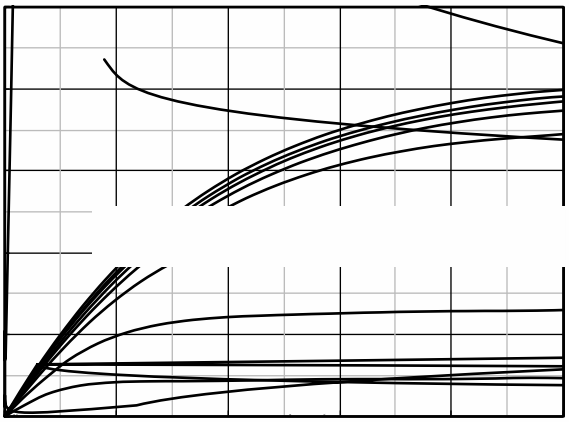
PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
BSS138AJKQ	F2	.SS	3000	30000	120000	7“ reel

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	50	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V, V_{GS}=0V	-	-	1	μA
		V_{DS}=50V, V_{GS}=0V, Tj=150	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±5	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	0.7	1	1.45	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=0.5A	-	1.2	1.6	Ω
		V_{GS}=4.5V, I_D=0.1A	-	1.24	2.5	
		V_{GS}=2.5V, I_D=0.1A	-	1.8	3.8	
Diode Forward Voltage	V_{SD}	I_S=0.22A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	75	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	0.22	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1MHz	-	29	-	pF
Output Capacitance	C_{oss}		-	4.3	-	
Reverse Transfer Capacitance	C_{rss}		-	3	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=25V, I_D=0.5A	-	1.2	-	nC
Gate-Source Charge	Q_{gs}		-	0.15	-	
Gate-Drain Charge	Q_{gd}		-	0.31	-	
Reverse Recovery Charge	Q_{rr}	I_F=0.5A, di/dt=100A/us	-	2.1	-	nC
Reverse Recovery Time	t_{rr}		-	9.2	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=25V, I_D=0.5A R_{GEN}=25Ω	-	3	-	ns
Turn-on Rise Time	t_r		-	2.7	-	
Turn-off Delay Time	$t_{D(off)}$		-	11	-	
Turn-off fall Time	t_f		-	8.1	-	

Note:
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with TA =25 .The maximum allowed junction temperature of 150 . The value in any given application depends on the user's specific board design.

■Typical Electrical and Thermal Characteristics Diagrams



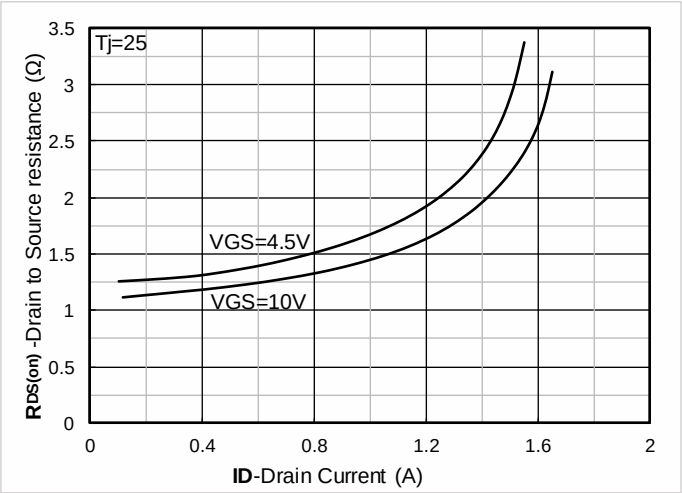


Figure 7. $R_{DS(on)}$ VS Drain Current

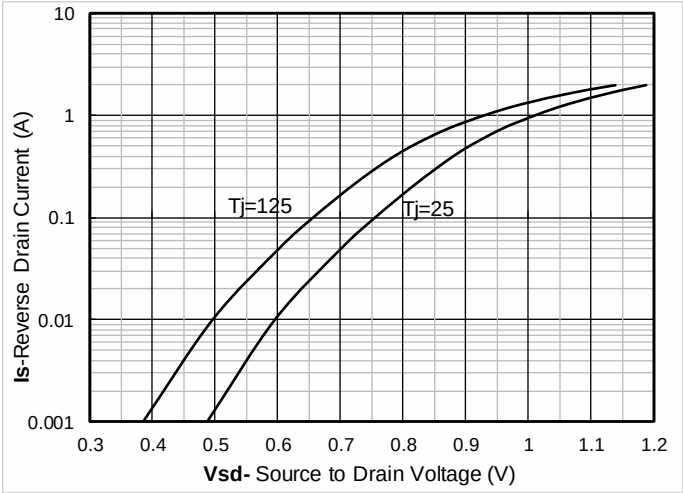
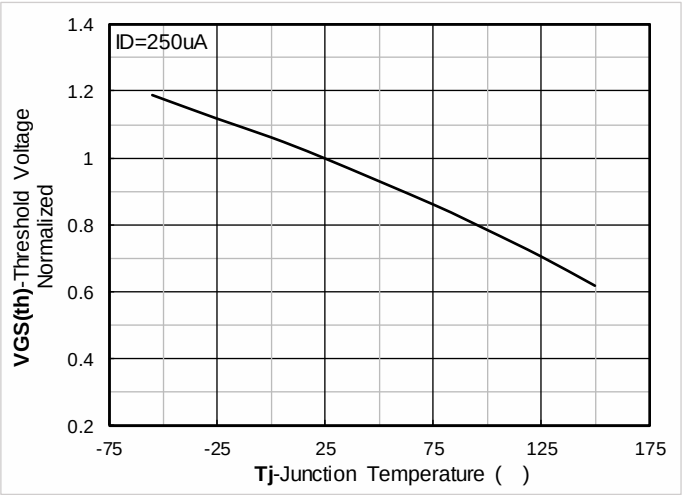
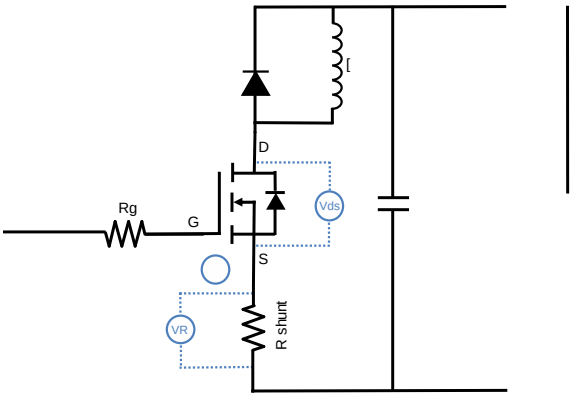
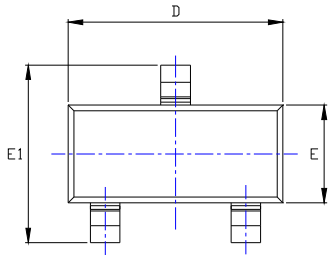


Figure 8. Forward characteristics of reverse diode

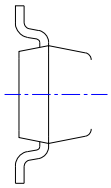



L
D
Rg
G
Vds
S
VR
R shunt

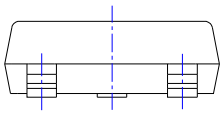
■ SOT-23 Package information



TOP VIEW



SIDE VIEW



UNIT mm

SUGGESTED SOLDER PAD LAYOUT

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